**What is Claimed is:**

1. A system of integrated circuit components defining a plurality of nodes and a random access memory (RAM) connected to each node, each node comprising:

at least one functional unit configured to carry out a predetermined processing function;

a communication mechanism configured to manage and control communication of information with other nodes;

a memory controller configured to control writes to and reads from the RAM connected to the node;

wherein the system is further configured to permit read access to a RAM by a plurality of the nodes in the system, but is further configured to limit write access to a RAM to only the node to which the RAM is connected.

2. The system of claim 1, wherein the system is a computer graphics system.

3. The system of claim 1, wherein the at least one functional unit is one selected from the group consisting of a texture mapping component, a geometry accelerator, a shader, a z/blend component, a rasterizer, a tiler, and a cache controller.

4. The system of claim 1, wherein each node further includes control means for controlling the use and access of memory storage by remote functional units.

5. The system of claim 4, wherein the control means includes a memory segment containing at least one work queue, the work queue being in the form of a first-in-first-out instruction queue for the at least one functional unit.

6. The system of claim 5, wherein the work queue contains a plurality of messages.

7. The system of claim 6, wherein messages may be communicated between different nodes under control of the control means.

8. The system of claim 1, wherein the plurality of nodes are interconnected via a plurality of serial communication links.

9. The system of claim 4, wherein the RAM is segmented to include at least one segment dedicated to the control means of the connected node and at least one additional segment dedicated to carrying out a functional operation of the system.

10. The system of claim 9, wherein the RAM is segmented to further include at least one additional segment dedicated to a portion of a texture map surface and a portion of an image surface, and the remaining texture map surface and image surface are stored in memory segments of RAMs connected to other nodes, wherein the various texture map surface segments and image surface segments are partitioned and stored among the RAMs in a non-duplicative manner.

11. A system of integrated circuit components comprising:

a plurality of nodes interconnected by communication links;

a random access memory (RAM) connected to each node;

at least one functional unit integrated into each node, each functional unit configured to carry out a predetermined processing function;

each node containing a coherency mechanism configured to permit only read access to the RAM by other nodes, the coherency mechanism further configured to permit write access to the RAM only by functional units that are local to the node.

12. The system of claim 11, wherein a work queue comprises at least one message, the at least one message containing an instruction of the at least one functional unit of the associated node.

13. The system of claim 12, wherein messages may be communicated between different nodes under control of the control means.

14. The system of claim 13, wherein the plurality of nodes are interconnected via a plurality of serial communication links.